WHAT IS CLAIMED IS:

1. A semiconductor device, comprising a polysilicon gate electrode provided on a silicon substrate, wherein

said gate electrode is subjected to compressive stress as internal stress therein, to apply tensile stress to said silicon substrate, and

ions having a mass number of 70 or more are implanted into said gate electrode.

2. The semiconductor device according to claim 1, wherein

said gate electrode is a gate electrode of an n-channel MOS transistor.

3. The semiconductor device according to claim 2, wherein

said ions having a mass number of 70 or more are operative to serve as those for forming a source and drain region of said n-channel MOS transistor.

4. The semiconductor device according to claim 1, wherein

said ions having a mass number of 70 or more are electrically inactive ions.

5. The semiconductor device according to claim 1, wherein

said gate electrode has a bird's beak at a lower edge portion thereof, said bird's beak being defined by a silicon oxide film.

6. The semiconductor device according to claim 1, wherein

said silicon substrate is a strained silicon substrate.

7. A method of manufacturing a semiconductor device, comprising the steps of:

(a) providing a non-single crystalline silicon gate electrode on a silicon substrate;

(b) implanting ions having a mass number of 70 or more into said gate electrode;

(c) depositing a predetermined film at a temperature of 550 $\circ C$ or less, to cover said gate electrode including therein said ions having a mass number of 70 or more; and

(d) performing thermal processing at a temperature of more than 550 $\circ C$ while covering said gate electrode with said predetermined film.

8. The method according to claim 7, wherein

said gate electrode is a gate electrode of an n-channel MOS transistor.

9. The method according to claim 7, wherein

said gate electrode provided in said step (a) includes a plurality of gate electrodes, and

only a predetermined one of said plurality of gate electrodes undergoes said step (b).

10. The method according to claim 9, wherein

said plurality of gate electrodes include gate electrodes of an n-channel MOS transistor and a p-channel MOS transistor, and

said predetermined one of said plurality of gate electrodes to be subjected to

said step (b) is a gate electrode of said n-channel MOS transistor.

11. The method according to claim 9, wherein

said plurality of gate electrode include gate electrodes of a plurality of n-channel MOS transistors.

12. The method according to claim 7, wherein

said gate electrode provided in said step (a) includes a plurality of gate electrodes,

said method further comprising the step of:

(e) prior to said step (d), removing a part of said predetermined film on a predetermined one of said plurality of gate electrodes.

13. The method according to claim 8, wherein

ion implantation at said step (b) is intended to form a source and drain region of said n-channel MOS transistor.

14. The method according to claim 7, wherein

said ions implanted at said step (b) are electrically inactive ions.

15. The method according to claim 7, wherein

said predetermined film has a property that it shrinks by said thermal processing.

16. The method according to claim 7, wherein

said predetermined film is a silicon oxide film.

17. The method according to claim 7, further comprising:

(f) oxidizing surfaces of said silicon substrate and said gate electrode, to form a bird's beak defined by a silicon oxide film at a lower edge portion of said gate electrode.

18. The method according to claim 7, wherein

said silicon substrate is a strained silicon substrate.